



# MX575ABD800M000

## Ultra-Low Jitter 800MHz HCSL XO

### ClockWorks® FUSION

### General Description

The MX575ABD800M000 is an ultra-low phase jitter XO with HCSL output optimized for high line rate applications.

### Features

- 800MHz HCSL
- Typical phase noise:
  - 85fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

### Absolute Maximum Ratings<sup>1</sup>

Supply Voltage (VIN).....	+4.6V
Lead Temperature (soldering, 10s).....	260°C
Case Temperature.....	115°C
Storage Temperature (T <sub>g</sub> ).....	-65°C to +125°C
ESD Machine Model.....	200V
ESD Rating (HBM).....	2kV

### Operating Ratings<sup>2</sup>

Supply Voltage (VIN).....	+2.375V to +3.63V
Ambient Temperature (TA).....	-40°C to +85°C
Junction Thermal Resistance	
LGA (T <sub>JA</sub> ) Still Air.....	53°C/W

### Electrical Characteristics

VDD = 2.5V ±5% or 3.3V ±10%, -40°C to +85°C, outputs terminated with 50 Ohms to VSS.<sup>3</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				95	mA
F0	Center Frequency			800		MHz
	Frequency Stability	Note 4			±50	ppm
∅j	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		185 85		fsRMS
Tstart	Start-Up Time				10	ms
TR/TF	Rise/Fall time	20%-80%	150	300	450	ps
	Duty Cycle		48	50	52	%
VOH	Output High Voltage	HCSL output levels	660	700	850	mV
VOL	Output Low Voltage	HCSL output levels	-150	0	27	mV
VOVS	Max Output Including Overshoot				VOH + 0.3	V
VUDS	Min Output Including Undershoot		VOL - 0.3			V
VRB	Ringback Voltage		0.2			V
VOX	Absolute Crossing Point		250	350	550	mV
Vswing	Peak to Peak Output Voltage Swing		640	700	950	mV

#### Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Guaranteed after thermal equilibrium.
4. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

ClockWorks is a registered trademark of Microchip Technology Inc.

## Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX575ABD800M000	MX575AB	D800M000	Tube	6-Pin 7mm x 5mm LGA
MX575ABD800M000-TR	MX575AB	D800M000	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

## Pin Configuration



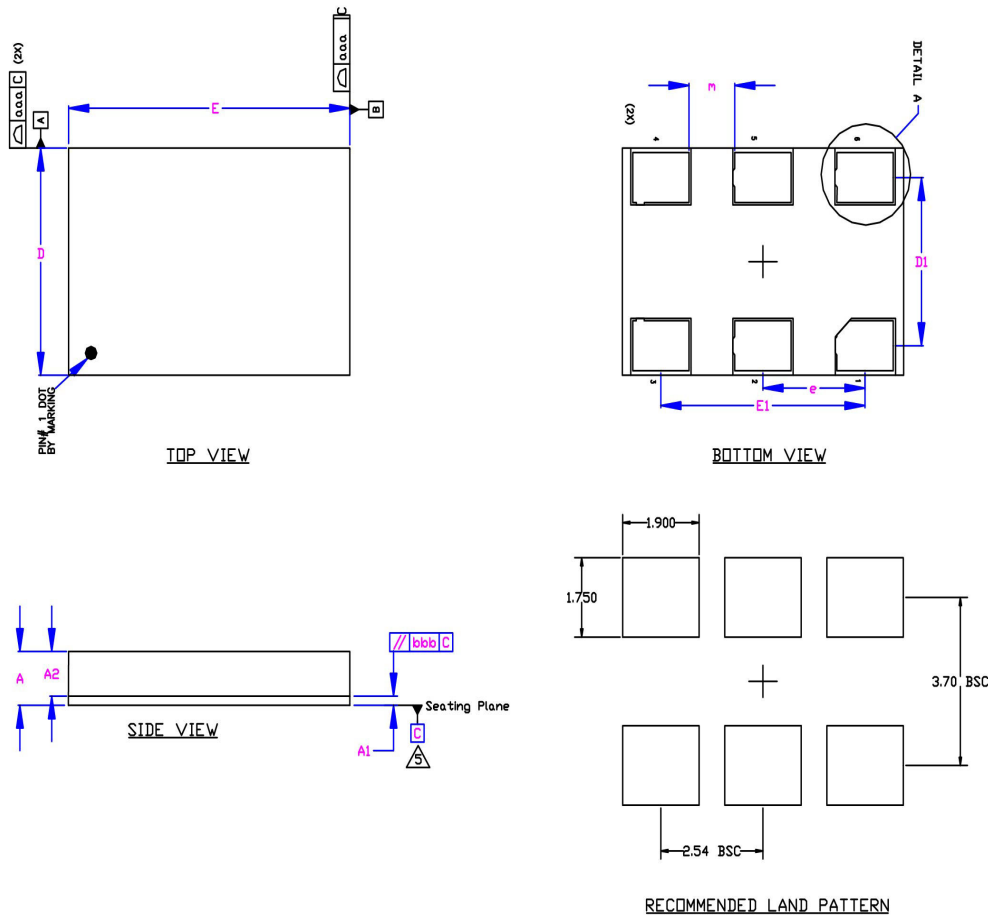
## Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	HCSL	Clock Output Frequency = 800MHz
6	VDD	PWR		Power Supply

## Environmental Specifications

Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2002, Condition C
Mechanical Vibration	MIL-STD-883, Method 2007, Condition B
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)
Hazardous Substance	Pb-Free / RoHS / Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1=2x10 <sup>-8</sup> atm cc/s
Solvent Resistance	MIL-STD-202, Method 215

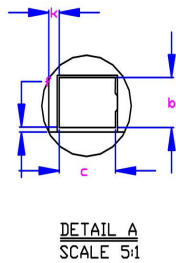
### Package Information and Recommended Land Pattern for 6-Pin LGA<sup>3</sup>



Dimensional Tol.	
aaa	0.100
bbb	0.070

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.260	1.330	1.400
A1	0.190	0.230	0.270
A2	1.070	1.100	1.130
D	4.900	5.000	5.100
D1	3.700 BSC		
E	6.900	7.000	7.100
E1	5.000 BSC		
b	1.050	1.100	1.150
c	1.350	1.400	1.450
e	2.540 BSC		
f	0.050	0.100	0.150
k	0.210	0.260	0.310
m	1.090	1.140	1.190
n	36		



- Notes
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
  2. Dimensions are in millimeters.
  3. 'e' represents the basic LGA pitch
  4. 'n' is the maximum no. of Land for a specified Package.
  5. Package warp shall be 0.150 max.
  6. Substrate base is BT Resin
  7. The Pin#1 corner must be identified on top side only.
  8. Reference Jeduc Spec M1-221
  9. Land pattern tolerance is 0.05mm unless otherwise specified

#### 6-Pin LGA (7x5mm)

Note:  
3. Package information is correct as of the publication date. For updates and most current information, go to [www.microchip.com](http://www.microchip.com).

Microchip Technology Inc.

<http://www.microchip.com>

Microchip makes no representations or warranties with respect to the accuracy or completeness of the information furnished in this data sheet. This information is not intended as a warranty and Microchip does not assume responsibility for its use. Microchip reserves the right to change circuitry, specifications and descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Microchip's terms and conditions of sale for such products, Microchip assumes no liability whatsoever, and Microchip disclaims any express or implied warranty relating to the sale and/or use of Microchip products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right.

© 2017 Microchip Technology Inc.