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December 2015

FDB0105N407L

N-Channel PowerTrench[®] MOSFET

40 V, 460 A, 0.8 mΩ

Features

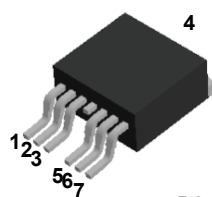
- Max $r_{DS(on)}$ = 0.8 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 50\text{ A}$
- Max $r_{DS(on)}$ = 1.1 mΩ at $V_{GS} = 6\text{ V}$, $I_D = 42\text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench[®] process that has been especially tailored to minimize the on-state resistance while maintaining superior ruggedness and switching performance for industrial applications.

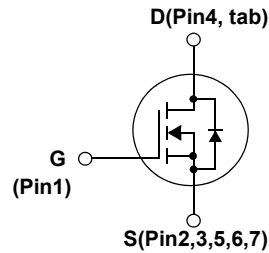
Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch



1. Gate
2. Source/Kelvin Sense
3. Source/Kelvin Sense
4. Drain
5. Source
6. Source
7. Source

D2-PAK
(TO263)



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous	$T_C = 25^\circ\text{C}$ (Note 5)	460
	-Continuous	$T_C = 100^\circ\text{C}$ (Note 5)	330
	-Pulsed	(Note 4)	2540
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	1109
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	300
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	3.8
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	0.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB0105N407L	FDB0105N407L	D2-PAK-7L	330mm	24mm	800 units

FDB0105N407L N-Channel PowerTrench[®] MOSFET

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		13		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2	2.8	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 50\ \text{A}$		0.6	0.8	m Ω
		$V_{GS} = 6\ \text{V}, I_D = 42\ \text{A}$		0.8	1.1	
		$V_{GS} = 10\ \text{V}, I_D = 50\ \text{A}, T_J = 150^\circ\text{C}$		1	1.8	
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}, I_D = 50\ \text{A}$		286		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		16500	23100	pF
C_{oss}	Output Capacitance			5335	7470	pF
C_{rss}	Reverse Transfer Capacitance			973	1365	pF
R_g	Gate Resistance			2.6		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\ \text{V}, I_D = 50\ \text{A}, V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		45	73	ns
t_r	Rise Time			69	110	ns
$t_{d(off)}$	Turn-Off Delay Time			117	186	ns
t_f	Fall Time			61	97	ns
Q_g	Total Gate Charge			208	291	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 20\ \text{V}, I_D = 50\ \text{A}, V_{GS} = 10\ \text{V}$		64		nC
Q_{gd}	Gate to Drain "Miller" Charge			29		nC

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	460	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	2540	A
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 50\ \text{A}$ (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 50\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		107	171	ns
Q_{rr}	Reverse Recovery Charge			119	191	nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

- a) $40^\circ\text{C}/\text{W}$ when mounted on a $1\ \text{in}^2$ pad of 2 oz. copper.
 b) $62.5^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.

3. E_{AS} of 1109 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.3\ \text{mH}$, $I_{AS} = 86\ \text{A}$, $V_{DD} = 10\ \text{V}$, $V_{GS} = 36\ \text{V}$. 100% test at $L = 0.1\ \text{mH}$, $I_{AS} = 125\ \text{A}$.

4. Pulsed I_d please refer to Figure "Forward Bias Safe Operating Area" for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

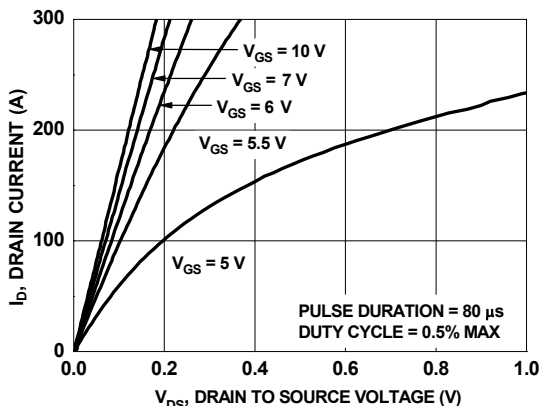


Figure 1. On Region Characteristics

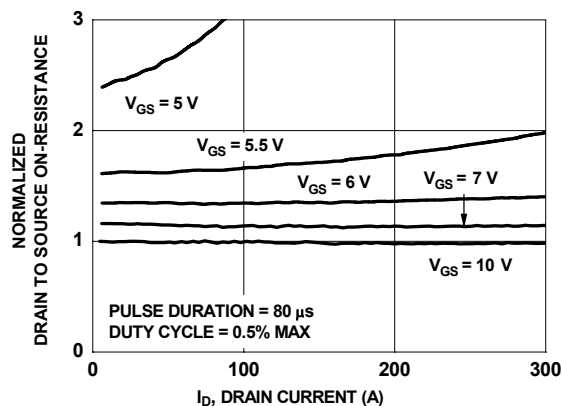


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

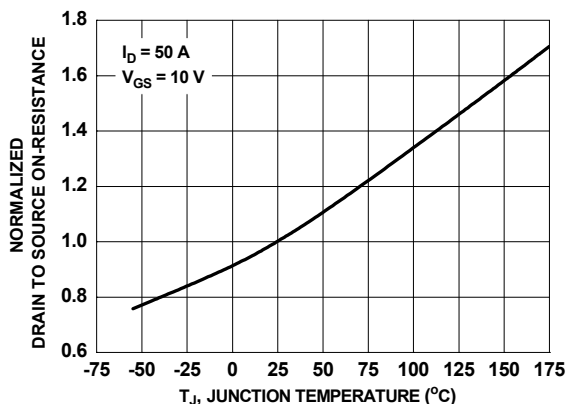


Figure 3. Normalized On Resistance vs. Junction Temperature

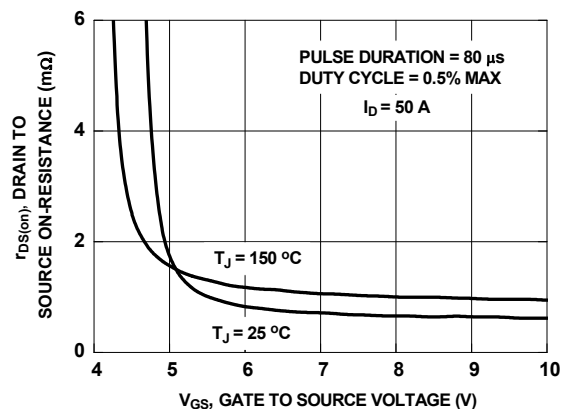


Figure 4. On-Resistance vs. Gate to Source Voltage

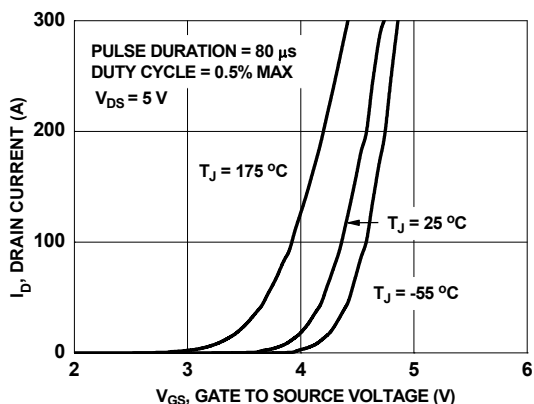


Figure 5. Transfer Characteristics

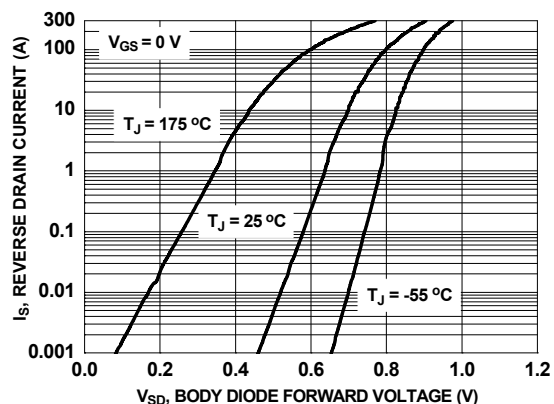


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

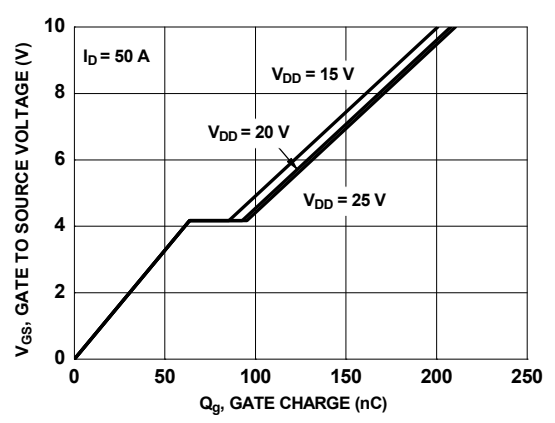


Figure 7. Gate Charge Characteristics

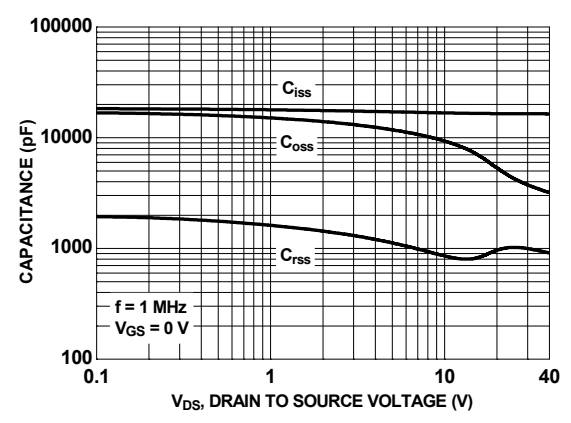


Figure 8. Capacitance vs. Drain to Source Voltage

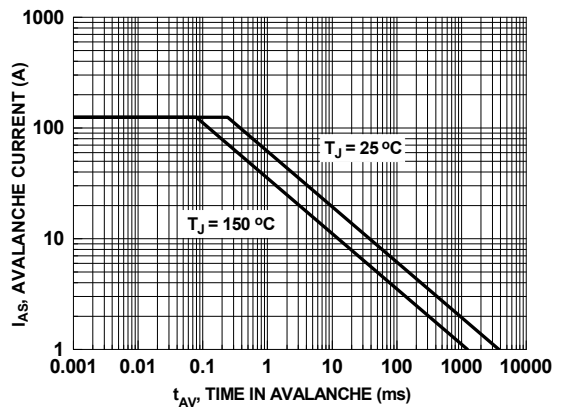


Figure 9. Unclamped Inductive Switching Capability

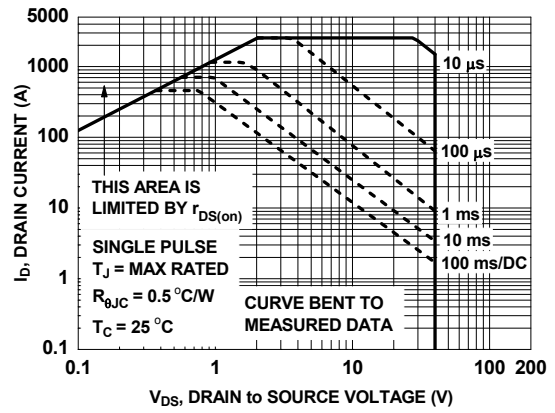


Figure 10. Forward Bias Safe Operating Area

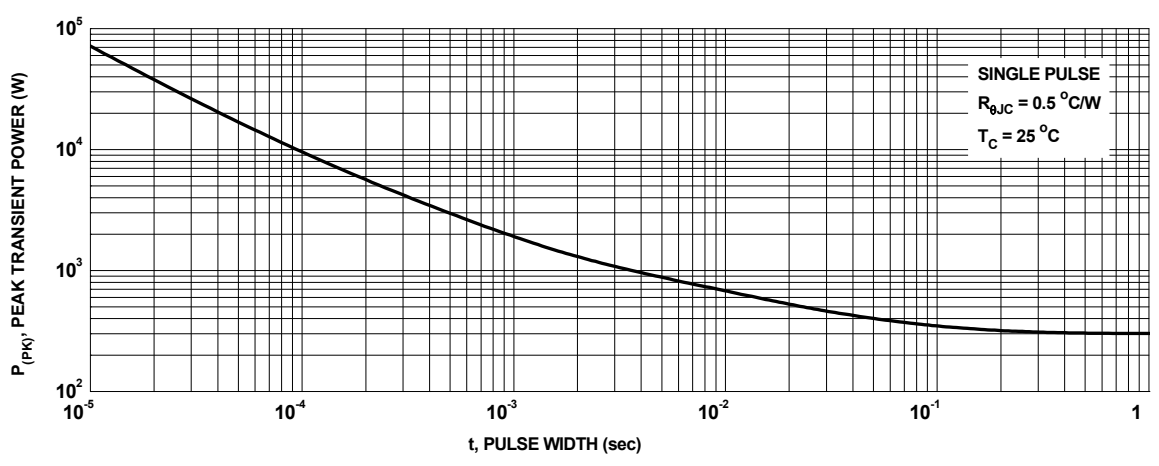


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

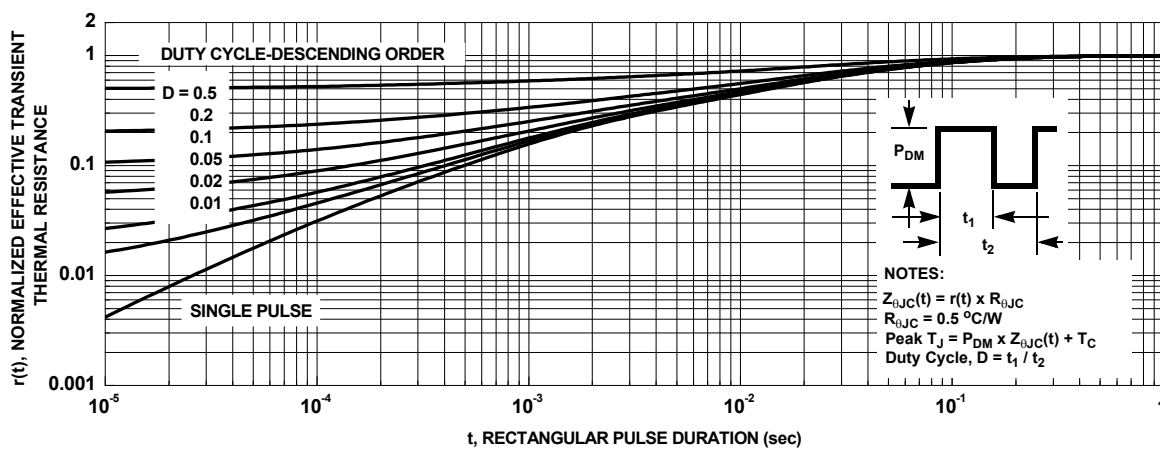
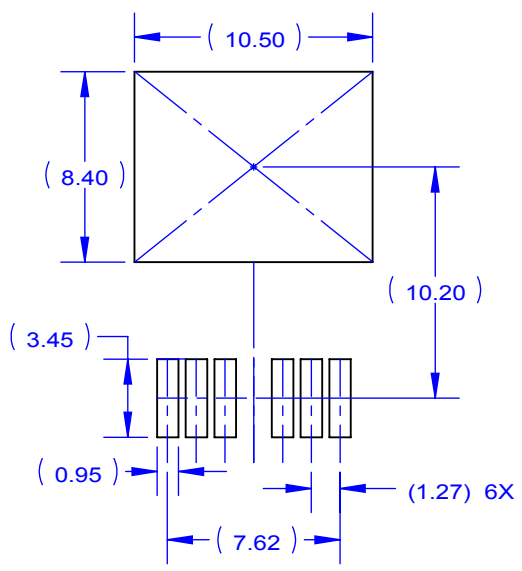
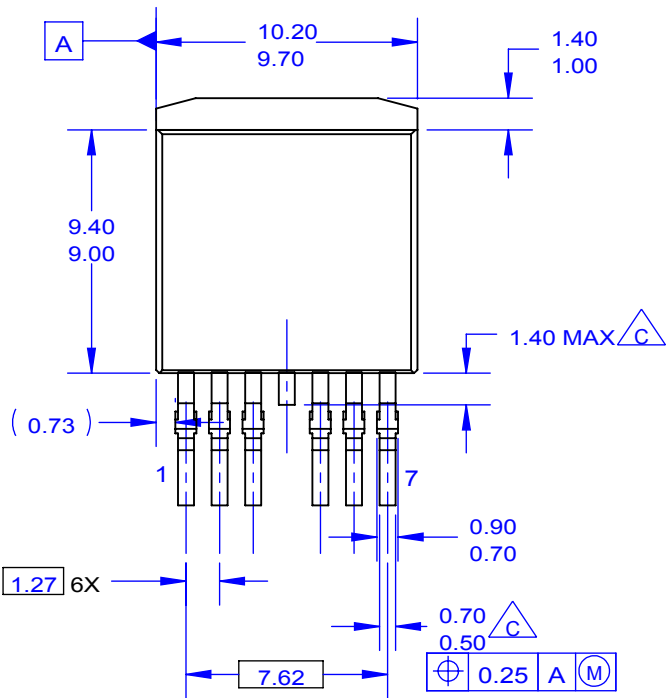
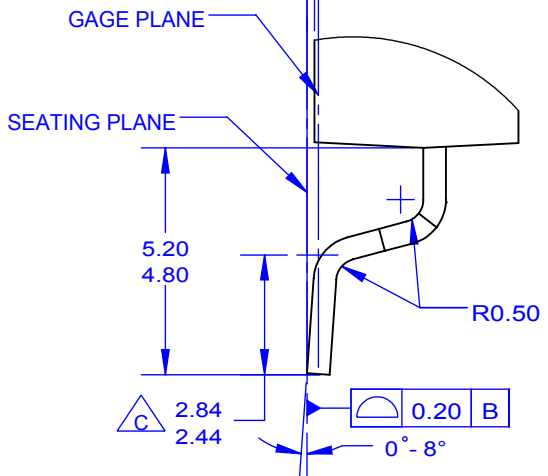
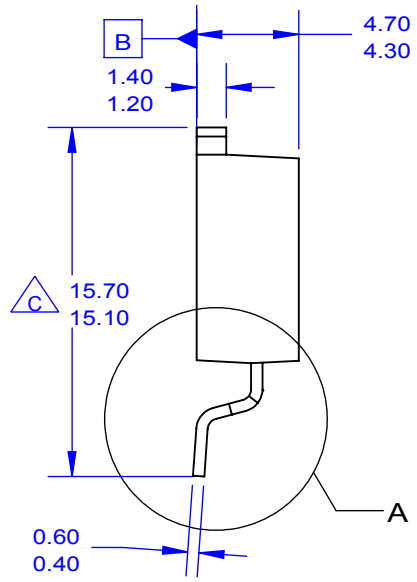
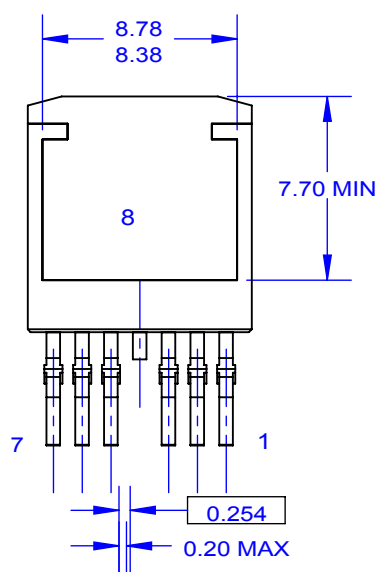


Figure 12. Junction-to-Case Transient Thermal Response Curve



LAND PATTERN RECOMMENDATION



DETAIL A
SCALE 2:1

NOTES:

- A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- $\triangle C$ OUT OF JEDEC STANDARD VALUE.
- D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- F. LAND PATTERN RECOMMENDATION PER IPC TO127P1524X465-8N.
- G. DRAWING FILE NAME: TO263A07REV5.

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