Ordering number : ENA1741A

LV5230BG

Bi-CMOS IC

7ch×17ch LED Driver

ON Semiconductor®

http://onsemi.com

Overview

The LV5230BG is a dot-matrix LED driver IC for cell phones.

Features

- 7×17 dot-matrix LED driver
  (5×15 dot-matrix supported)
- Each dot can be set for display over the serial bus.

Functions

- LED driver
  Column (anode) driving P-channel driver × 17 channels
  Row (cathode) driving N-channel driver × 7 channels
  LED current per dot : 25mA maximum
  Two flames of 7×17 (5×15) patterns can be set.
  7 grayscale level adjustment on a dot basis (PWM duty factor switching)
  Reverse display
  Horizontal scroll (1 frame/2 frames)
  Continuous/single scroll selectable
  Vertical scroll (1 frame/2 frames)
  Continuous/single scroll selectable
  Automatic flashing can be specified per each dot
  Interupt output at the end of scroll
  Ring tone synchronization function
- LED driving open drain output × 2

August, 2013

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max1	SV_{CC}, V_{DD}	5.5	V
	V_{CC} max2	$LEDV_{DD}$	6	V
Allowable power dissipation	Pd max	Mounted on a board *	1.15	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-40 to +125	°C

* Designated board : 40mm×50mm×0.8mm, glass epoxy 4-layter board (2S2P)

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{BAT}	SV_{CC}	3 to 4.5	V
Supply voltage 2	V_{DD}	V_{DD}	1.65 to 3	V
Supply voltage 3	$VLEDV_{DD}$	$LEDV_{DD}$	2.7 to 5.5	V

* Power application sequence : 1. V_{BAT} 2. V_{DD} $V_{BAT} > V_{DD}$, No restriction on $VLEDV_{DD}$.

* Same level of voltage $LEDV_{CC}$ must be applied to the 4 pins as $VLEDV_{DD}$ voltage.

Electrical Characteristics, Analog Block Ta = 25°C, V_{BAT} = 3.7V, V_{DD} = 2.6V, $LEDV_{DD}$ = 3.7V, unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Consumption current (SV_{CC}+V_{DD}+$LEDV_{DD}$)						
Consumption current 1	$I_{CC}1$	RESET : L		0	5	μA
Consumption current 2	$I_{CC}2$	RESET : H, serial default		0.3	5	μA
Consumption current 3A	$I_{CC}3A$	When STBY mode is released, RT external resistance value is 27kΩ		1.9	3	mA
Consumption current 3B	$I_{CC}3B$	When STBY mode is released, RT external resistance value is 160kΩ		1	2	mA
LEDSW						
On resistance 1	Ron1	ROW1 to 7 : IL = 425mA		1	2	Ω
On resistance 2	Ron2	LEDO1, LED02 : IL = 20mA		2	4	Ω
LED current 1	ILED1	COL1 to COL17 : V_O = $LEDV_{DD}$-0.5V RT external resistance value : 27kΩ	20	22.5	25	mA
LED current 2	ILED2	COL1 to COL17 : V_O = $LEDV_{DD}$-0.5V RT external resistance value : 160kΩ	2.8	3.8	4.8	mA
Leakage current 1	IL1	ROW1 to ROW : V_O = 5V			1	μA
Leakage current 2	IL2	COL1 to COL17 : V_O = 0V, $LEDV_{DD}$ = 5V			1	μA
Leakage current 3	IL3	LEDO1, LED02 : V_O = 5V			1	μA
OSC						
Oscillator frequency	F1	When RT external resistance is 27kΩ, CT external capacitance is 120pF	900	1000	1100	kHz
Oscillator frequency	F1	When RT external resistance is 160kΩ, CT external capacitance is 10pF	900	1000	1100	kHz
RT						
Maximum. LED drive current setting	LI1	RT external resistance : 27kΩ LED maximum drive current = 607.5/RT resistance	20	22.5	25	mA

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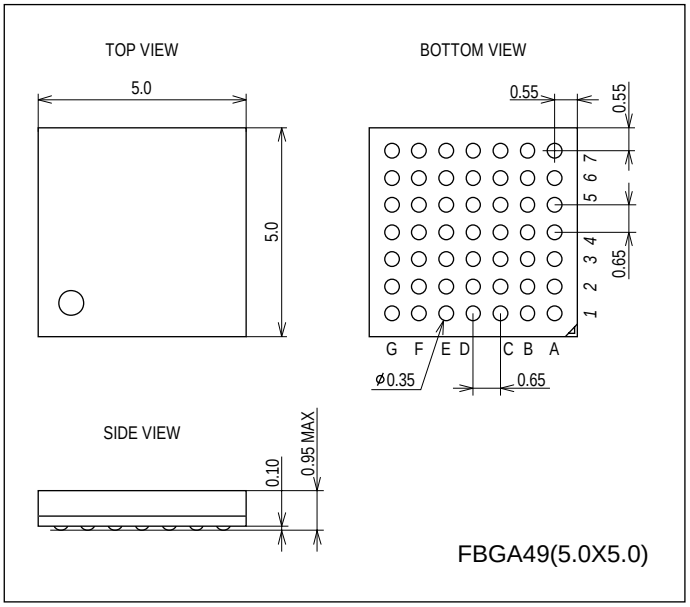
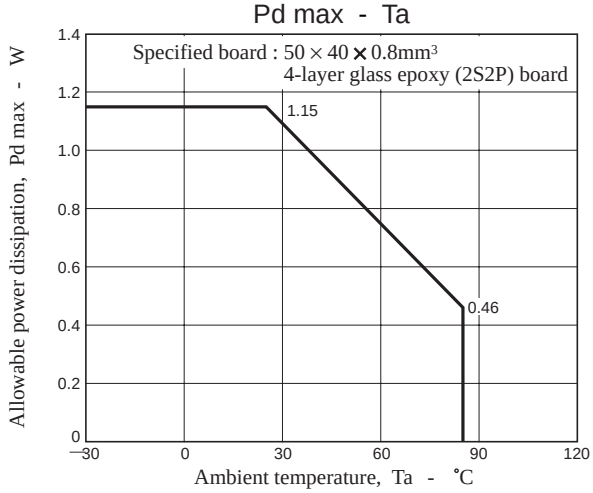
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Control Circuit Block						
H level 1	$V_{INH}1$	Input H level, SDA, SCL	V_{DD}×0.8			V
L level 1	$V_{INL}1$	Input L level, SDA, SCL	0		V_{DD}×0.2	V
H level 2	$V_{INH}2$	Input H level, RESET, SCTL	1.5			V
L level 2	$V_{INL}2$	Input L level, RESET, SCTL	0		0.3	V
H input current 3	$I_{HIN}3$	Inflow-outflow current, when VBAT voltage is applied to RESET pin.	-1	0	1	µA
L input current 3	$I_{LIN}3$	Inflow-outflow current, when 0V is applied to RESET pin.	-1	0	1	µA
H input current 4	$I_{HIN}4$	Inflow-outflow current, when VBAT voltage is applied to SCTL pin.	15	47	75	µA
L input current 4	$I_{LIN}4$	Inflow-outflow current, when 0V is applied to SCTL pin.	-1	0	1	µA
H output level 1	VH1	INTO pin, H level, I_O = 1mA	V_{DD}-0.3		V_{DD}	V
L output level 1	VL1	INTO pin, L level, I_O = 1mA	0		0.3	V

Package Dimensions

unit : mm (typ)

3396





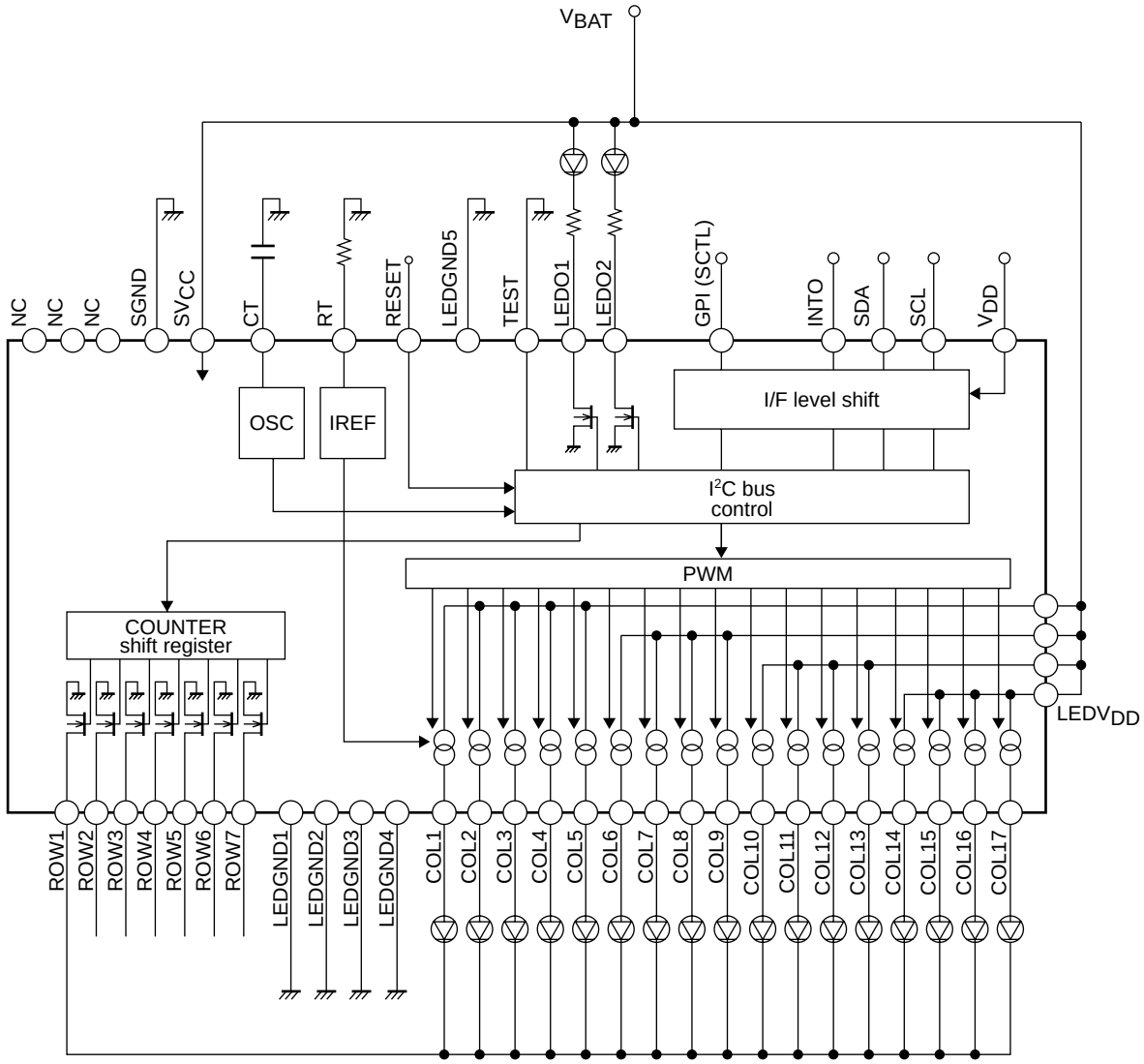
Pin Assignment

Top view

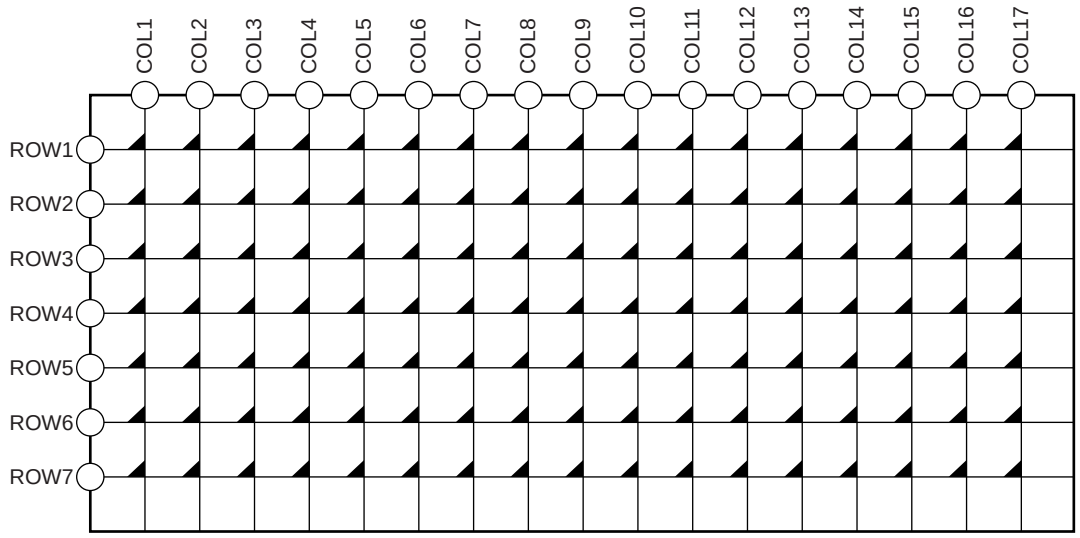
	G	F	E	D	C	B	A	
1	NC	COL16	CT	**SGND**	**LEDGND 1**	ROW2	TEST	1
2	**$LEDV_{DD}$**	COL17	**SV_{CC}**	SDA	ROW1	ROW3	RT	2
3	COL15	COL14	COL13	SCL	**V_{DD}**	**LEDGND 2**	ROW4	3
4	**$LEDV_{DD}$**	COL12	COL11	RESET	INTO	ROW5	**LEDGND 3**	4
5	COL10	COL9	COL4	COL2	GPI	ROW6	**LEDGND 4**	5
6	**$LEDV_{DD}$**	COL8	COL5	COL3	LEDO2	LEDO1	ROW7	6
7	NC	COL7	COL6	**$LEDV_{DD}$**	COL1	**LEDGND 5**	NC	7
	G	F	E	D	C	B	A	

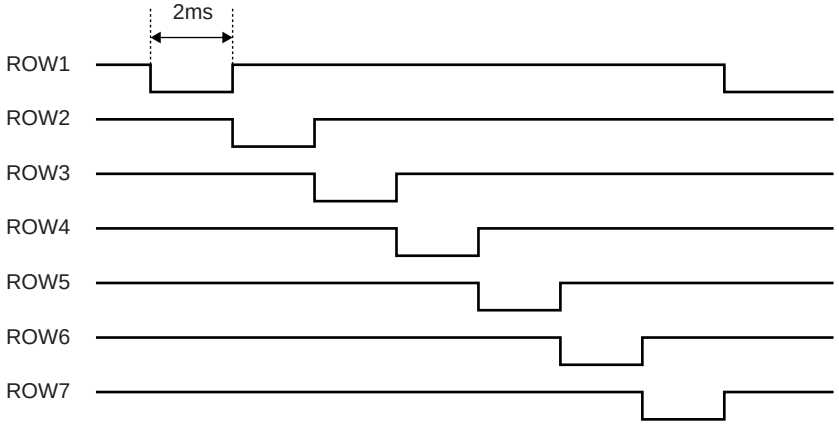
Grid	PIN NAME	Function	Protection diode vs. $LEDV_{DD}$	Protection diode vs. SV_{CC}	Protection diode vs. GND
A1	TEST	TEST input pin		○	○
A2	RT	Standard current setting resistance connection pin			○
A3	ROW4	ROW SW4	○		○
A4	LEDGND3	ROW SW GND			
A5	LEDGND4	ROW SW GND			
A6	ROW7	ROW SW7	○		○
A7	NC	No connection			
B1	ROW2	ROW SW2	○		○
B2	ROW3	ROW SW3	○		○
B3	LEDGND2	ROW SW GND			
B4	ROW5	ROW SW5	○		○
B5	ROW6	ROW SW6	○		○
B6	LEDO1	LED driver 1			○
B7	LEDGND5	LEDO1,2 exclusive GND			
C1	LEDGND1	ROW SW GND	-	-	-
C2	ROW1	ROW SW1	○		○
C3	V_{DD}	Serial I/O supply voltage		○	○
C4	INTO	INT output		○	○
C5	GPI	Receiving melody synchronous signal input pin		○	○
C6	LEDO2	LED driver 2			○
C7	COL1	COL SW1	○		○
D1	SGND	Analog logic GND			
D2	SDA	Serial data signal input			○
D3	SCL	Serial clock signal input			○
D4	RESET	Reset pin		○	○
D5	COL2	COL SW2	○		○
D6	COL3	COL SW3	○		○
D7	$LEDV_{DD}$	Dot matrix LED drive voltage impression pin			
E1	CT	Setting of frequency of transmitter capacitor connection pin			○
E2	SV_{CC}	Analog logic supply voltage			
E3	COL13	COL SW13	○		○
E4	COL11	COL SW11	○		○
E5	COL4	COL SW4	○		○
E6	COL5	COL SW5	○		○
E7	COL6	COL SW6	○		○
F1	COL16	COL SW16	○		○
F2	COL17	COL SW17	○		○
F3	COL14	COL SW14	○		○
F4	COL12	COL SW12	○		○
F5	COL9	COL SW9	○		○
F6	COL8	COL SW8	○		○
F7	COL7	COL SW7	○		○
G1	NC	No connection			
G2	$LEDV_{DD}$	Dot matrix LED drive voltage impression pin			
G3	COL15	COL SW15	○		○
G4	$LEDV_{DD}$	Dot matrix LED drive voltage impression pin			
G5	COL10	COL SW10	○		○
G6	$LEDV_{DD}$	Dot matrix LED drive voltage impression pin			
G7	NC	No connection			

Block Diagram



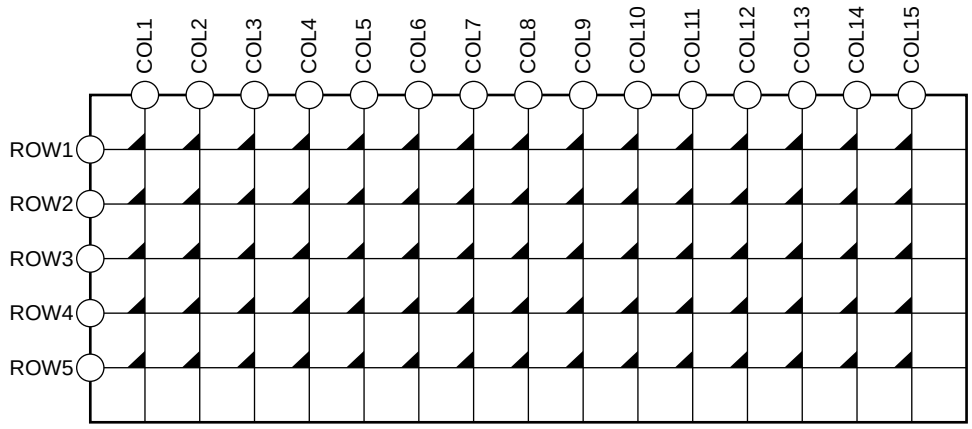
Dot Matrix LED 7 × 17

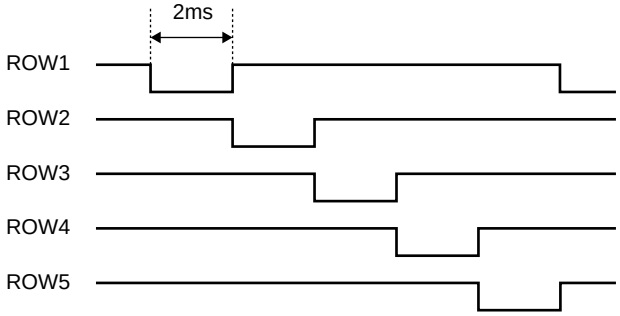




Dynamic Display

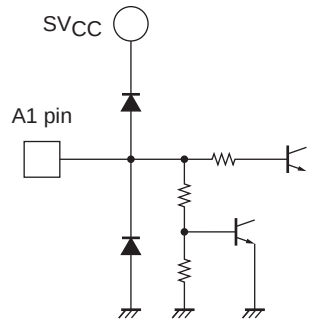
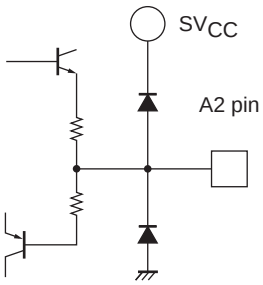
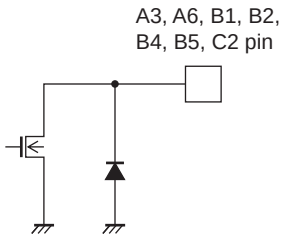
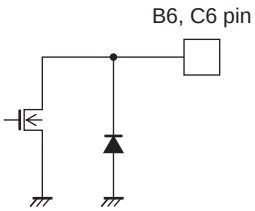
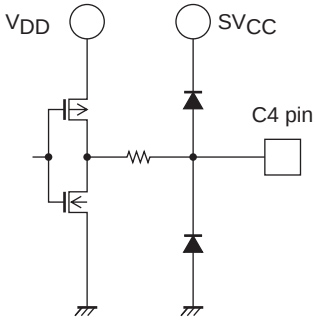
Dot Matrix LED 5 × 15





Dynamic Display

Pin Functions

Pin No.	Pin name	Pin Description	Equivalent Circuit
A1	TEST	Test signal input pin. Be sure to connect the pin to GND.	
A2	RT	Reference current setting resistor connection pin. By connecting the external resistor between this pin and GND, the reference current is generated. The pin voltage is about 0.61V. Change of this current value enables change of the oscillation frequency and LED driver current value (COL1 to COL17 only).	
A3 A6 B1 B2 B4 B5 C2	ROW4 ROW7 ROW2 ROW3 ROW5 ROW6 ROW1	N-channel driver output pins 1 to 7 for row (cathode) drive. Must be connected to GND when not to be used.	
A4	LEDGND3	ROW SW GND.	
A5	LEDGND4	ROW SW GND.	
A7 G1 G7	NC	No connection.	
B3	LEDGND2	ROW SW GND.	
B6 C6	LEDO1 LEDO2	Open drain output pins for LED drive. Must be connected to GND when not to be used.	
B7	LEDGND5	GND pin dedicated for LEDO1 and LEDO2.	
C1	LEDGND1	ROW SW GND.	
C3	V_{DD}	Power supply for serial I/F.	
C4	INTO	Interrupt signal output pin.	

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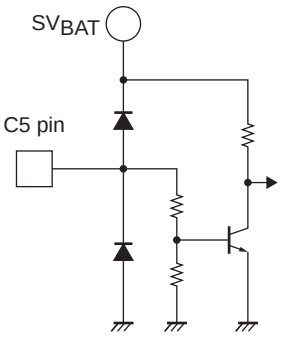
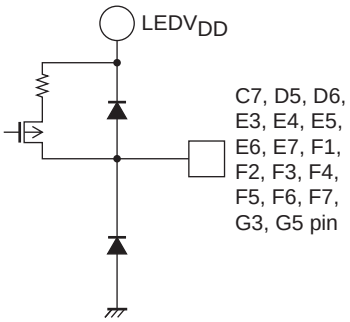
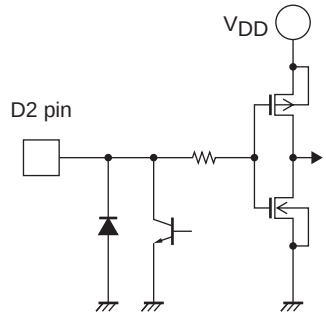
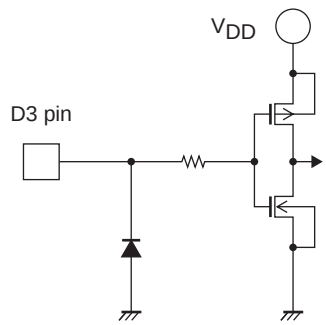
Pin No.	Pin name	Pin Description	Equivalent Circuit
C5	GPI	Ringing tone synchronization signal input pin. Must be connected to GND when not to be used.	
C7 D5 D6 E3 E4 E5 E6 E7 F1 F2 F3 F4 F5 F6 F7 G3 G5	COL1 COL2 COL3 COL13 COL11 COL4 COL5 COL6 COL16 COL17 COL14 COL12 COL9 COL8 COL7 COL15 COL10	P-channel driver output pins 1 to 17 for column (anode) drive. Must be connected to GND when not to be used.	
D7 G2 G4 G6	$LEDV_{DD}$	Dot matrix LED drive voltage supply pins.	
D1	SGND	Analog circuit GND pin.	
D2	SDA	Serial data signal input pin.	
D3	SCL	Serial clock signal input pin.	

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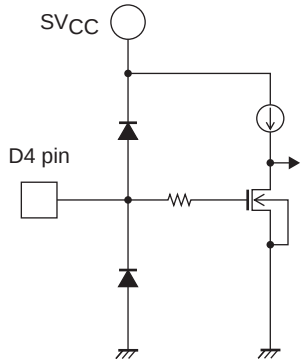
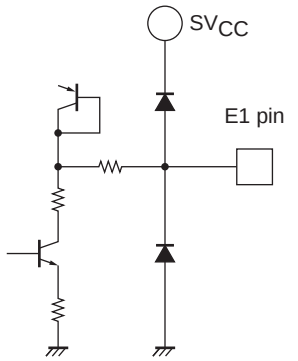
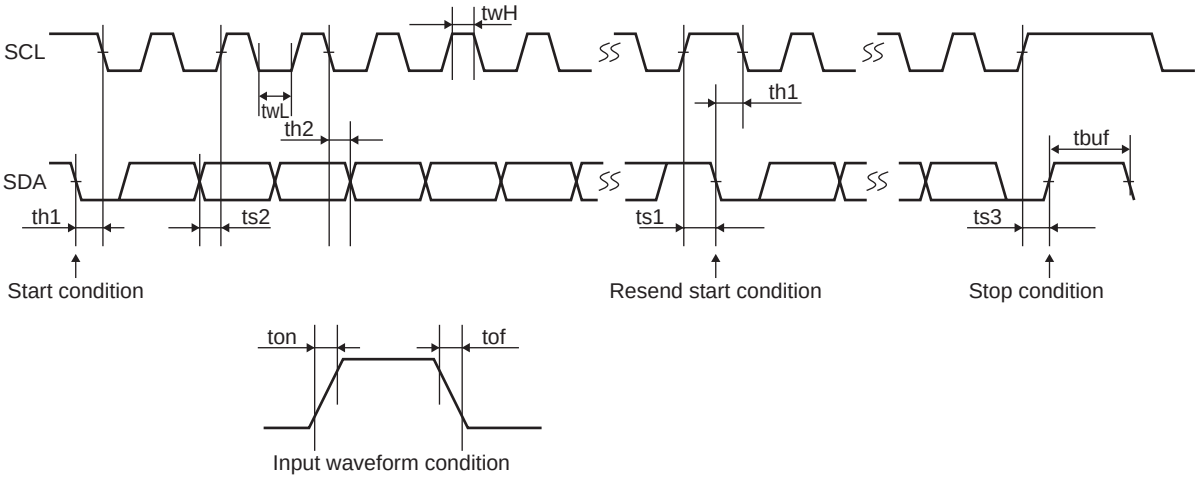
Pin No.	Pin name	Pin Description	Equivalent Circuit
D4	RESET	Reset signal input pin. Reset state when low.	
E1	CT	Oscillator frequency setting capacitor connection pin. The oscillation frequency can be adjusted by changing the value of capacitor at CT pin.	
E2	SV_{CC}	Analog circuit power supply.	

Serial Bus Communication Specifications

I²C serial transfer timing conditions



Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		100	kHz
Data set up time	ts1	SCL setup time relative to the fall of SDA	4.7			µs
	ts2	SDA setup time relative to the rise of SCL	250			ns
	ts3	SCL setup time relative to the rise of SDA	4.0			µs
Data hold time	th1	SCL data hold time relative to the fall of SDA	4.0			µs
	th2	SDA hold time relative to the fall of SCL	0			µs
Pulse width	twL	SCL pulse width for the L period	4.7			µs
	twH	SCL pulse width for the H period	4.0			µs
Input waveform conditions	ton	SCL and SDA (input) rise time			1000	ns
	tof	SCL and SDA (input) fall time			300	ns
Bus free time	tbuf	Time between STOP and START conditions	4.7			µs

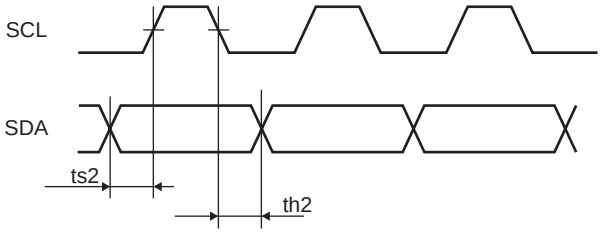
High-speed mode

Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		400	kHz
Data setup time	ts1	SCL setup time relative to the fall of SDA	0.6			µs
	ts2	SDA setup time relative to the rise of SCL	100			ns
	ts3	SCL setup time relative to the rise of SDA	0.6			µs
Data hold time	th1	SCL data hold time relative to the fall of SDA	0.6			µs
	th2	SDA hold time relative to the fall of SCL	0			µs
Pulse width	twL	SCL pulse width for the L period	1.3			µs
	twH	SCL pulse width for the H period	0.6			µs
Input waveform conditions	ton	SCL and SDA (input) rise time			300	ns
	tof	SCL and SDA (input) fall time			300	ns
Bus free time	tbuf	Time between STOP and START conditions	1.3			µs

I²C bus transmission method

Start and stop conditions

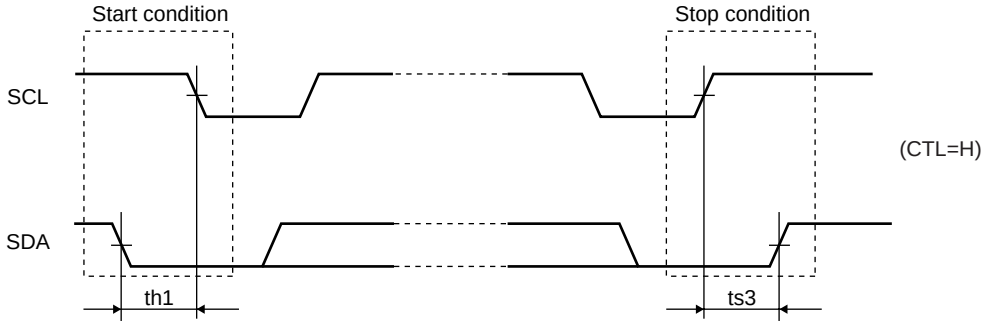
In the I²C bus, SDA must basically be kept in the constant state while SCL is “H” as shown below during data transfer.



When data transfer is not made, both SCL and SDA are in the “H” state.

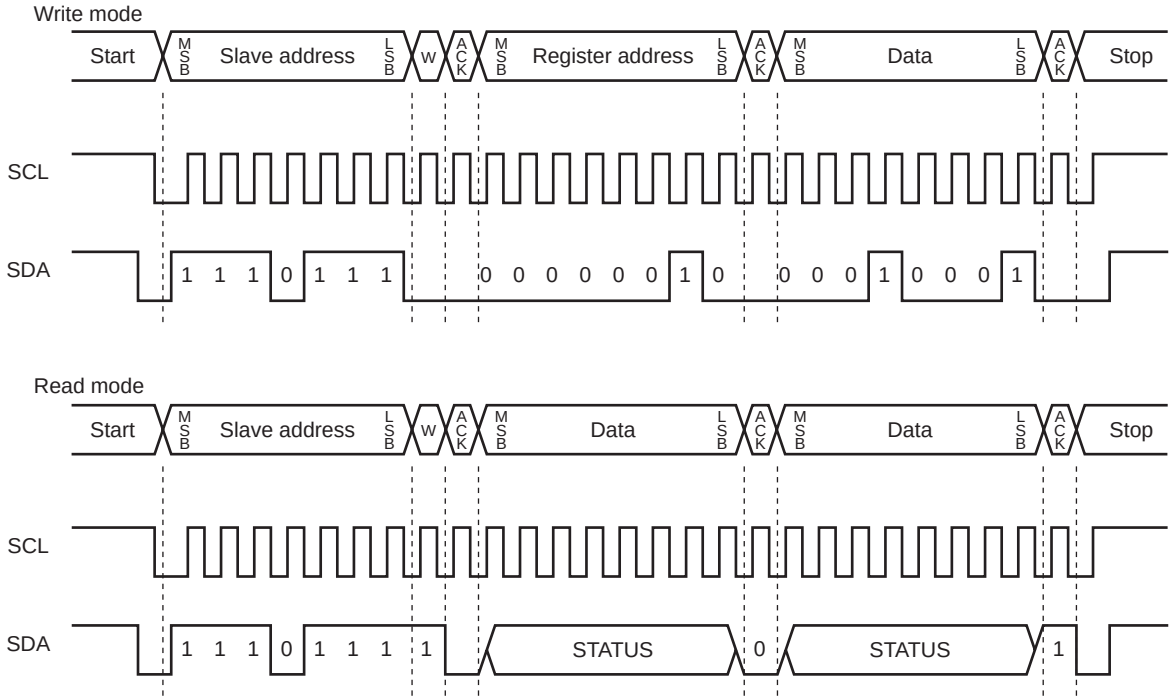
When SCL = SDA = “H”, change of SDA from “H” to “L” enables the start conditions to start access.

When SCL is “H”, change of SDA from “L” to “H” enables the stop conditions to stop access.



Data transfer and acknowledgement response

After establishment of start conditions, data transfer is made by one byte (8 bits).
Data transfer enables continuous transfer of any number of bytes.
Each time the 8-bit data is transferred, the ACK signal is sent from the receive side to the send side.
The ACK signal is issued when SDA on the send side is released and SDA on the receive side is set “L” immediately after fall of the clock pulse at the SCL eighth bit of data transfer to “L”.
When the next 1-byte transfer is left in the receive state after transmission of the ACK signal from the receive side, the receive side releases SDA at fall of the SCL ninth clock.
In the I^2C bus, there is no CE signal. Instead, 7-bit slave address is assigned to each device and the first byte of transfer is assigned to the command (R/W) representing the 7-bit slave address and subsequent transfer direction.
The 7-bit address is transferred sequentially from MSB and if the eighth bit is “L”, the second byte is WRITE mode and if “H”, the second byte is READ mode.
In the READ mode, the ACK signal issued immediately before sending the stop condition must be 1.
In LV5230, the slave address is specified as (1110111).



Serial modes setting

address : 00h CTRL1

00h CTRL1	D7	D6	D5	D4	D3	D2	D1	D0
Register name	STBY	-	MXMODE	MSWEN	-	DFCLR	FADECLR	SCRLCLR
R/W	W		W	W		W	W	W
Default	0		0	0		0	0	0

D0 : SCRLCLR Scroll interrupt signal clear
0 : Scroll interrupt signal stays active.
1 : Scroll interrupt signal cleared. * Automatically updated to 0 after being set to 1.

D1 : FADECLR Fade interrupt signal clear
0 : Fade interrupt signal stays active.
1 : Fade interrupt signal cleared. * Automatically updated to 0 after being set to 1.

D2 : DFCLR Pallete fade interrupt signal clear
0 : Pallete fade interrupt signal stays active.
1 : Pallete fade interrupt signal cleared. * Automatically updated to 0 after being set to 1.

D4 : MSWEN Ringing tone synchronization enable
0 : Ringing tone synchronization enabled. * GPI = L : All LEDs turned off, GPI = H : Normal operation
1 : Ringing tone synchronization disabled.

D5 : MXMODE LED matrix mode switchingr
0 : 7 × 17 LED matrix
1 : 5 × 15 LED matrix

D7: STBY Standby mode
0 : Standby
1 : Operation

address : 01h CTRL2

01h CTRL2	D7	D6	D5	D4	D3	D2	D1	D0
Register name	LEDOFF	-	LED2	LED1	-	ROTHEN	ROTVEN	PAGE
R/W	W		W	W		W	W	W
Default	0		0	0		0	0	0

D0 : PAGE Display page
0 : Frame 1 displayed
1 : Frame 2 displayed

D1 : ROTVEN Vertical rotation
0 : Normal display
1 : Vertically rotated display

D2 : ROTHEN Horizontal rotation
0 : Normal display
1 : Horizontally rotated display

D4 : LED1 LED1 enable
0 : LED1 turned off
1 : LED1 turned on

D5 : LED2 LED2 enable
0 : LED2 turned off
1 : LED2 turned on

D7 : LEDOFF Screen display ON/OFF
0 : Normal operation
1 : All matrix LEDs turned off

address : 02h DOTMODE

02h DOTMODE	D7	D6	D5	D4	D3	D2	D1	D0
Register name	DOTEN	DOTMODE	-	-	DOTSP [3]	DOTSP [2]	DOTSP [1]	DOTSP [0]
R/W	W	W			W	W	W	W
Default	0	0			0	0	0	0

D3-D0 : DOTSP Flashing/brightness inversion speed

D3	D2	D1	D0		
0	0	0	0	ON : 0.05s	OFF : 0.05s
0	0	0	1	ON : 0.10s	OFF : 0.10s
0	0	1	0	ON : 0.15s	OFF : 0.15s
0	0	1	1	ON : 0.20s	OFF : 0.20s
0	1	0	0	ON : 0.25s	OFF : 0.25s
0	1	0	1	ON : 0.30s	OFF : 0.30s
0	1	1	0	ON : 0.35s	OFF : 0.35s
0	1	1	1	ON : 0.40s	OFF : 0.40s
1	0	0	0	ON : 0.45s	OFF : 0.45s
1	0	0	1	ON : 0.50s	OFF : 0.50s
1	0	1	0	ON : 0.55s	OFF : 0.55s
1	0	1	1	ON : 0.60s	OFF : 0.60s
1	1	0	0	ON : 0.65s	OFF : 0.65s
1	1	0	1	ON : 0.70s	OFF : 0.70s
1	1	1	0	ON : 0.75s	OFF : 0.75s
1	1	1	1	ON : 0.80s	OFF : 0.80s

D6 : DOTMODE Flashing/brightness inversion display switching

0 : Flashing

1 : Brightness inversion

D7 : DOTEN Flashing/brightness inversion display enable

0 : Disable

1 : Enable

address : 03h AUTOPAGE

03h AUTOPAGE	D7	D6	D5	D4	D3	D2	D1	D0
Register name	PGEN	-	-	-	PGSP [3]	PGSP [2]	PGSP [1]	PGSP [0]
R/W	W				W	W	W	W
Default	0				0	0	0	0

D3 top D0 : PGSP Page switching speed

D3	D2	D1	D0		
0	0	0	0	Page1 : 0.05s	Page2 : 0.05s
0	0	0	1	Page1 : 0.10s	Page2 : 0.10s
0	0	1	0	Page1 : 0.15s	Page2 : 0.15s
0	0	1	1	Page1 : 0.20s	Page2 : 0.20s
0	1	0	0	Page1 : 0.25s	Page2 : 0.25s
0	1	0	1	Page1 : 0.30s	Page2 : 0.30s
0	1	1	0	Page1 : 0.35s	Page2 : 0.35s
0	1	1	1	Page1 : 0.40s	Page2 : 0.40s
1	0	0	0	Page1 : 0.45s	Page2 : 0.45s
1	0	0	1	Page1 : 0.50s	Page2 : 0.50s
1	0	1	0	Page1 : 0.55s	Page2 : 0.55s
1	0	1	1	Page1 : 0.60s	Page2 : 0.60s
1	1	0	0	Page1 : 0.65s	Page2 : 0.65s
1	1	0	1	Page1 : 0.70s	Page2 : 0.70s
1	1	1	0	Page1 : 0.75s	Page2 : 0.75s
1	1	1	1	Page1 : 0.80s	Page2 : 0.80s

D7 : PGEN Automatic page switching enable

0 : Disable

1 : Enable

address : 04h SCCON1

04h SCCON1	D7	D6	D5	D4	D3	D2	D1	D0
Register name	SCEN	SCDIR [1]	SCDIR [0]	SCMODE	SCSP [3]	SCSP [2]	SCSP [1]	SCSP [0]
R/W	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

D3 to D0 : SCSP Scroll speed per dot

D3	D2	D1	D0	
0	0	0	0	50ms
0	0	0	1	100ms
0	0	1	0	150ms
0	0	1	1	200ms
0	1	0	0	250ms
0	1	0	1	300ms
0	1	1	0	350ms
0	1	1	1	400ms
1	0	0	0	450ms
1	0	0	1	500ms
1	0	1	0	550ms
1	0	1	1	600ms
1	1	0	0	650ms
1	1	0	1	700ms
1	1	1	0	750ms
1	1	1	1	800ms

D4 : SCMODE Page mode when scrolling

0 : Scrolls and displays the current page repeatedly.

1 : Scrolls and displays the current and other pages alternately.

D6 to D5 : SCDIR Scroll direction

D6	D5	
0	0	Right
0	1	Left
1	0	Up
1	1	Down

D7 : SCEN Scroll enable

0 : Disable

1 : Enable

address : 05h SCCON2

05h SCCON2	D7	D6	D5	D4	D3	D2	D1	D0
Register name	SCGO	-	SCCNT [5]	SCCNT [4]	SCCNT [3]	SCCNT [2]	SCCNT [1]	SCCNT [0]
R/W	W		W	W	W	W	W	W
Default	0		0	0	0	0	0	0

D0 to D5 : SCCNT Scroll increment

17 × 7 mode

When SCCON1.SCDIR = 0 or 1 : 1 to 34

When SCCON1.SCDIR = 2 or 3 : 1 to 14

15 × 5 mode

When SCCON1.SCDIR = 0 or 1 : 1 to 30

When SCCON1.SCDIR = 2 or 3 : 1 to 10

* Scrolls one page when SCCNT = 0.

D7 : SCGO Scroll start

0 : Standby

1 : Scroll start

* The scrolled state is maintained until SCCON1 and SCEN are set low.

address : 06h FADECON

06h FADECON	D7	D6	D5	D4	D3	D2	D1	D0
Register name	FADEEN	FADEGO	FADEIO	FADEMOD	FDSP [3]	FDSP [2]	FDSP [1]	FDSP [0]
R/W	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

D3 to D0 : FDSP Fade speed per 1 grayscale level (It takes (following set value × 64) seconds to complete fading)

D3	D2	D1	D0	
0	0	0	0	2ms
0	0	0	1	4ms
0	0	1	0	6ms
0	0	1	1	8ms
0	1	0	0	10ms
0	1	0	1	12ms
0	1	1	0	14ms
0	1	1	1	16ms
1	0	0	0	18ms
1	0	0	1	20ms
1	0	1	0	22ms
1	0	1	1	24ms
1	1	0	0	26ms
1	1	0	1	28ms
1	1	1	0	30ms
1	1	1	1	32ms

D4 : FADEMOD Single/continuous switching
0 : Single fade-in/fade-out operation
1 : Fade-in/fade-out operation repeated

D5 : FADEIO Fade-in/fade-out switching
0 : Fade in
1 : Fade out

D6 : FADEGO Fade-in/fade-out start
0 : Standby
1 : Fade-in/fade-out operation start

D7 : FADEEN Fade-in/fade-out enable
0 : Disable
1 : Enable

* The interrupt flag is set high after a fade operation has completed. Manual clearing is required.
* All LEDs are turned off if FADEEN is set to 1 when FADEO is set to 0.
If GO is set to 1 in that state, fade-in operation starts and LEDs are turned on.

address : 07h ROWSW

07h ROWSW	D7	D6	D5	D4	D3	D2	D1	D0
Register name	ROWSWEN	ROWSW7	ROWSW6	ROWSW5	ROWSW4	ROWSW3	ROWSW2	ROWSW1
R/W	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

D0 : ROWSW1 Row 1 display ON/OFF
0 : ON
1 : OFF

D1 : ROWSW2 Row 2 display ON/OFF
0 : ON
1 : OFF

D2 : ROWSW3 Row 3 display ON/OFF
0 : ON
1 : OFF

D3 : ROWSW4 Row 4 display ON/OFF
0 : ON
1 : OFF

D4 : ROWSW5 Row 5 display ON/OFF
0 : ON
1 : OFF

D5 : ROWSW6 Row 6 display ON/OFF
0 : ON
1 : OFF

D6 : ROWSW7 Row 7 display ON/OFF
0 : ON
1 : OFF

D7 : ROWSWEN Each row ON/OFF enable
0 : Disable
1 : Enable

address : 08h COLSW1

08h COLSW1	D7	D6	D5	D4	D3	D2	D1	D0
Register name	COLSWEN	-	-	-	-	-	-	COLSW17
R/W	W							W
Default	0							0

D0 : COLSW17 Row 17 display ON/OFF
0 : ON
1 : OFF

D7 : COLSWEN Column ON/OFF enable
0 : Disable
1 : Enable

address : 09h COLSW2

09h COLSW2	D7	D6	D5	D4	D3	D2	D1	D0
Register name	COLSW16	COLSW15	COLSW14	COLSW13	COLSW12	COLSW11	COLSW10	COLSW9
R/W	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

D0 : COLSW9 Column 9 display ON/OFF
0 : ON
1 : OFF

D1 : COLSW10 Column 10 display ON/OFF
0 : ON
1 : OFF

D2 : COLSW11 Column 11 display ON/OFF
0 : ON
1 : OFF

D3 : COLSW12 Column 12 display ON/OFF
0 : ON
1 : OFF

D4 : COLSW13 Column 13 display ON/OFF
0 : ON
1 : OFF

D5 : COLSW14 Column 14 display ON/OFF
0 : ON
1 : OFF

D6 : COLSW15 Column 15 display ON/OFF
0 : ON
1 : OFF

D7 : COLSW16 Column 16 display ON/OFF
0 : ON
1 : OFF

address : 0Ah COLSW3

0Ah COLSW3	D7	D6	D5	D4	D3	D2	D1	D0
Register name	COLSW8	COLSW7	COLSW6	COLSW5	COLSW4	COLSW3	COLSW2	COLSW1
R/W	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

D0 : COLSW1 Column 1 display ON/OFF
0 : ON
1 : OFF

D1 : COLSW2 Column 2 display ON/OFF
0 : ON
1 : OFF

D2 : COLSW3 Column 3 display ON/OFF
0 : ON
1 : OFF

D3 : COLSW4 Column 4 display ON/OFF
0 : ON
1 : OFF

D4 : COLSW5 Column 5 display ON/OFF
0 : ON
1 : OFF

D5 : COLSW6 Column 6 display ON/OFF
0 : ON
1 : OFF

D6 : COLSW7 Column 7 display ON/OFF
0 : ON
1 : OFF

D7 : COLSW8 Column 8 display ON/OFF
0 : ON
1 : OFF

address : 0Bh DFCON1

0Bh DFCON1	D7	D6	D5	D4	D3	D2	D1	D0
Register name	DFEN	DFGO	-	-	DFDIR	DFNUM [2]	DFNUM [1]	DFNUM [0]
R/W	W	W			W	W	W	W
Default	0	0			0	0	0	0

D2 to D0 : DFNUM Number of palette to be faded to
0 : Invalid
1 to 7 : Correspond to PWMDUTY1 to PWMDUTY7.

D3 : DFDIR Fading direction
0 : Fade in
1 : Fade out

D6 : DFGO Fade start
0 : Standby
1 : Start

D7 : DFEN Fade enable
0 : Disable
1 : Enable

* The interrupt flag is set high after a fade operation has completed. Manual clearing is required.

address : 0Ch DFCON2

0Ch DFCON2	D7	D6	D5	D4	D3	D2	D1	D0
Register name	-	-	-	-	DFSP [3]	DFSP [2]	DFSP [1]	DFSP [0]
R/W					W	W	W	W
Default					0	0	0	0

D3 to D0 : DFSP Fading speed per grayscale

D3	D2	D1	D0	
0	0	0	0	2ms
0	0	0	1	4ms
0	0	1	0	6ms
0	0	1	1	8ms
0	1	0	0	10ms
0	1	0	1	12ms
0	1	1	0	14ms
0	1	1	1	16ms
1	0	0	0	18ms
1	0	0	1	20ms
1	0	1	0	22ms
1	0	1	1	24ms
1	1	0	0	26ms
1	1	0	1	28ms
1	1	1	0	30ms
1	1	1	1	32ms

address : 0Dh MAXDUTY

0Dh MAXDUTY	D7	D6	D5	D4	D3	D2	D1	D0
Register name	-	-	MXDTY [5]	MXDTY [4]	MXDTY [3]	MXDTY [2]	MXDTY [1]	MXDTY [0]
R/W			W	W	W	W	W	W
Default			0	0	0	0	0	0

D5 to D0 : MXDTY Maximum DUTY value

n : 0 to 63 Maximum DUTY value (n/64) × 100[%]

* 100[%] when n = 63.

address : 10h PWMDUTY1

10h PWMDUTY1	D7	D6	D5	D4	D3	D2	D1	D0
Register name	-	-	DUTY1 [5]	DUTY1 [4]	DUTY1 [3]	DUTY1 [2]	DUTY1 [1]	DUTY1 [0]
R/W			W	W	W	W	W	W
Default			0	0	0	0	0	0

D5 to D0 : DUTY1 DUTY value for brightness 1 setting

n : 0 to 63 DUTY value ((n + 1)/64) × 100 [%]

* 0 [%] when n = 0.

address : 11h PWMDUTY2

11h PWMDUTY2	D7	D6	D5	D4	D3	D2	D1	D0
Register name	-	-	DUTY2 [5]	DUTY2 [4]	DUTY2 [3]	DUTY2 [2]	DUTY2 [1]	DUTY2 [0]
R/W			W	W	W	W	W	W
Default			0	0	0	0	0	0

D5 to D0 : DUTY2 DUTY value for brightness 2 setting

n : 0 to 63 DUTY value ((n + 1)/64) × 100 [%]

* 0 [%] when n = 0.

address : 12h PWMDUTY3

12h PWMDUTY3	D7	D6	D5	D4	D3	D2	D1	D0
Register name	-	-	DUTY3 [5]	DUTY3 [4]	DUTY3 [3]	DUTY3 [2]	DUTY3 [1]	DUTY3 [0]
R/W			W	W	W	W	W	W
Default			0	0	0	0	0	0

D5 to D0 : DUTY3 DUTY value for brightness 3 setting

n : 0 to 63 DUTY value ((n + 1)/64) × 100 [%]

* 0 [%] when n = 0.

address : 13h PWMDUTY4

13h PWMDUTY4	D7	D6	D5	D4	D3	D2	D1	D0
Register name	-	-	DUTY4 [5]	DUTY4 [4]	DUTY4 [3]	DUTY4 [2]	DUTY4 [1]	DUTY4 [0]
R/W			W	W	W	W	W	W
Default			0	0	0	0	0	0

D5 to D0 : DUTY4 DUTY value for brightness 4 setting

n : 0 to 63 DUTY value ((n + 1)/64) × 100 [%]

* 0 [%] when n = 0.

address : 14h PWMDUTY5

14h PWMDUTY5	D7	D6	D5	D4	D3	D2	D1	D0
Register name	-	-	DUTY5 [5]	DUTY5 [4]	DUTY5 [3]	DUTY5 [2]	DUTY5 [1]	DUTY5 [0]
R/W			W	W	W	W	W	W
Default			0	0	0	0	0	0

D5 to D0 : DUTY5 DUTY factor value for brightness 5 setting
n : 0 to 63 DUTY value $((n + 1)/64) \times 100$ [%]
* 0 [%] when n = 0.

address : 15h PWMDUTY6

15h PWMDUTY6	D7	D6	D5	D4	D3	D2	D1	D0
Register name	-	-	DUTY6 [5]	DUTY6 [4]	DUTY6 [3]	DUTY6 [2]	DUTY6 [1]	DUTY6 [0]
R/W			W	W	W	W	W	W
Default			0	0	0	0	0	0

D5 to D0 : DUTY6 DUTY factor value for brightness 6 setting
n : 0 to 63 DUTY value $((n + 1)/64) \times 100$ [%]
* 0 [%] when n = 0.

address : 16h PWMDUTY7

16h PWMDUTY7	D7	D6	D5	D4	D3	D2	D1	D0
Register name	-	-	DUTY7 [5]	DUTY7 [4]	DUTY7 [3]	DUTY7 [2]	DUTY7 [1]	DUTY7 [0]
R/W			W	W	W	W	W	W
Default			0	0	0	0	0	0

D5 to D0 : DUTY7 DUTY factor value for brightness 7 setting
n : 0 to 63 DUTY value $((n + 1)/64) \times 100$ [%]
* 0 [%] when n = 0.

address : 20h to 9Dh FRAMEDATA

20h to 9Dh FRAMEDATA	D7	D6	D5	D4	D3	D2	D1	D0
Register name	BRn	LMn [2]	LMn [1]	LMn [0]	BRm	LMm [2]	LMm [1]	LMm [0]
R/W	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

D2 to D0 : LM11m Frame 1 : vertical 1st : horizontal (n + 1) th LED brightness

D2	D1	D0	
0	0	0	Off
0	0	1	On at brightness set by PWMDUTY1 register
0	1	0	On at brightness set by PWMDUTY2 register
0	1	1	On at brightness set by PWMDUTY3 register
1	0	0	On at brightness set by PWMDUTY4 register
1	0	1	On at brightness set by PWMDUTY5 register
1	1	0	On at brightness set by PWMDUTY6 register
1	1	1	On at brightness set by PWMDUTY7 register

D3 : BR11m Frame 1 : vertical 1: horizontal (n + 1) th LED flashing/brightness inversion enable

0 : Flashing/brightness inversion disabled

1 : Flashing/brightness inversion enabled

D6 to D4 : LM11n Frame 1 : vertical 1 : horizontal (n) th LED brightness

D2	D1	D0	
0	0	0	Off
0	0	1	On at brightness set by PWMDUTY1 register
0	1	0	On at brightness set by PWMDUTY2 register
0	1	1	On at brightness set by PWMDUTY3 register
1	0	0	On at brightness set by PWMDUTY4 register
1	0	1	On at brightness set by PWMDUTY5 register
1	1	0	On at brightness set by PWMDUTY6 register
1	1	1	On at brightness set by PWMDUTY7 register

D7 : BR11n Frame 1 : vertical 1 : horizontal (n) th LED flashing/brightness inversion enable

0 : Flashing/brightness inversion disabled

1 : Flashing/brightness inversion enabled

* These are used for each LED data. One register is loaded with two LEDs data.
See the table on the following page for the storage address of each dot.

Frame Data Register Tables xxH : higher-order 4 bits of register xx xxL : lower-order 4 bits of register xx

17 × 7 mode

Frame 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	20H	20L	21H	21L	22H	22L	23H	23L	24H	24L	25H	25L	26H	26L	27H	27L	28H
2	29H	29L	2AH	2AL	2BH	2BL	2CH	2CL	2DH	2DL	2EH	2EL	2FH	2FL	30H	30L	31H
3	32H	32L	33H	33L	34H	34L	35H	35L	36H	36L	37H	37L	38H	38L	39H	39L	3AH
4	3BH	3BL	3CH	3CL	3DH	3DL	3EH	3EL	3FH	3FL	40H	40L	41H	41L	42H	42L	43H
5	44H	44L	45H	45L	46H	46L	47H	47L	48H	48L	49H	49L	4AH	4AL	4BH	4BL	4CH
6	4DH	4DL	4EH	4EL	4FH	4FL	50H	50L	51H	51L	52H	52L	53H	53L	54H	54L	55H
7	56H	56L	57H	57L	58H	58L	59H	59L	5AH	5AL	5BH	5BL	5CH	5CL	5DH	5DL	5EH

Frame 2

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	5FH	5FL	60H	60L	61H	61L	62H	62L	63H	63L	64H	64L	65H	65L	66H	66L	67H
2	68H	68L	69H	69L	6AH	6AL	6BH	6BL	6CH	6CL	6DH	6DL	6EH	6EL	6FH	6FL	70H
3	71H	71L	72H	72L	73H	73L	74H	74L	75H	75L	76H	76L	77H	77L	78H	78L	79H
4	7AH	7AL	7BH	7BL	7CH	7CL	7DH	7DL	7EH	7EL	7FH	7FL	80H	80L	81H	81L	82H
5	83H	83L	84H	84L	85H	85L	86H	86L	87H	87L	88H	88L	89H	89L	8AH	8AL	8BH
6	8CH	8CL	8DH	8DL	8EH	8EL	8FH	8FL	90H	90L	91H	91L	92H	92L	93H	93L	94H
7	95H	95L	96H	96L	97H	97L	98H	98L	99H	99L	9AH	9AL	9BH	9BL	9CH	9CL	9DH

15 × 5 mode

Frame 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	20H	20L	21H	21L	22H	22L	23H	23L	24H	24L	25H	25L	26H	26L	27H
2	29H	29L	2AH	2AL	2BH	2BL	2CH	2CL	2DH	2DL	2EH	2EL	2FH	2FL	30H
3	32H	32L	33H	33L	34H	34L	35H	35L	36H	36L	37H	37L	38H	38L	39H
4	3BH	3BL	3CH	3CL	3DH	3DL	3EH	3EL	3FH	3FL	40H	40L	41H	41L	42H
5	44H	44L	45H	45L	46H	46L	47H	47L	48H	48L	49H	49L	4AH	4AL	4BH

Frame 2

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	4DH	4DL	4EH	4EL	4FH	4FL	50H	50L	51H	51L	52H	52L	53H	53L	54H
2	56H	56L	57H	57L	58H	58L	59H	59L	5AH	5AL	5BH	5BL	5CH	5CL	5DH
3	5FH	5FL	60H	60L	61H	61L	62H	62L	63H	63L	64H	64L	65H	65L	66H
4	68H	68L	69H	69L	6AH	6AL	6BH	6BL	6CH	6CL	6DH	6DL	6EH	6EL	6FH
5	71H	71L	72H	72L	73H	73L	74H	74L	75H	75L	76H	76L	77H	77L	78H

address : FFh STATUS

FFh STATUS	D7	D6	D5	D4	D3	D2	D1	D0
Register name	-	-	-	-	-	DFIF	FEDIF	SCRIF
R/W						R	R	R
Default	X	X	X	X	X			

D0 : SCRIF End of scroll interrupt occurrence flag
0 : No end of scroll interrupt has occurred.
1 : An end of scroll interrupt has occurred.
* The flag needs to be cleared manually (CTRL1.SCRLCLR).

D1 : FEDIF End of fade interrupt occurrence flag
0 : No end of fade interrupt has occurred.
1 : An end of fade interrupt has occurred.
* The flag needs to be cleared manually (CTRL1.FADECLR).

D2 : DFIF End of palette fade interrupt occurrence flag
0 : No end of palette fade interrupt has occurred.
1 : An end of palette fade interrupt has occurred.
* The flag needs to be cleared manually (CTRL1.DFCLR).

The OR of SCRIF, FEDIF and DFIF appear at the interrupt pin.

* The addresses used here are all dummy and not used in actual communications.